




# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

| APPLICATION NO.  | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|--|-------------|----------------------|---------------------|------------------|
| 10/645,650   | 08/20/2003  | Dennis R. Whittaker  | INSY0001C           | 8805             |
| 22862  | 7590        | 04/22/2004           | EXAMINER            |                  |
| GLENN PATENT GROUP<br>3475 EDISON WAY, SUITE L<br>MENLO PARK, CA 94025 |             |                      | JEAN PIERRE, PEGUY  |                  |
|  |             |                      | ART UNIT            | PAPER NUMBER     |
|  |             |                      | 2819                |                  |

DATE MAILED: 04/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

|                              |                               |                                  |   |
|------------------------------|-------------------------------|----------------------------------|---|
| <b>Office Action Summary</b> | Application No.<br>10/645,650 | Applicant(s)<br>WHITTAKER ET AL. |   |
|                              | Examiner<br>Peguy JeanPierre  | Art Unit<br>2819                 |  |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 20 August 2003.
- 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☐ Claim(s) 1-3, 5, 7-14, 16, 18 and 19 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Specification***

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

### ***Claim Objections***

2. Claim 9 is objected to because of the following informalities: In order to clarify the claimed language, it is suggested to change the dependency of claim 9 to read claim 8 instead of claim 17. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Art Unit: 2819

5. Claims 1-3, 5, 7, 11-14, 16, 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shaw et al. (USP 4,218,675) in view of Brandt (USP 6,121,912).

Shaw et al. disclose in Figure 1 an analog to digital converter that comprises an input circuit (analog input) a reference circuit (14), a first converter (comparator 12) that determines the most significant bits, a second converter (comparator 46) that determines the least significant bits; latch (44) that receives the output of the second comparator representative of the comparison of the input signal (analog input) with the reference voltage. Shaw et al. fail to teach a sample and hold circuit for storing the input signal; means to determine the most significant bit and the next most significant bit of the converter; a digital calibration circuit; a resistor string to provide the plurality of reference voltages.

Brandt discloses in Figure 1 an analog to digital converter that comprises a sample and hold circuit (10) for storing an input signal; a resistor string (16) which generates a plurality of reference voltages to a first converter (12) that produces most significant bits of digital data; a second converter (20) that produces least significant bits of the digital data; an error correction logic (28) for calibrating and improving the accuracy of the analog to digital converter. Brandt further discloses in Table 1 the state of the switches of the sample and hold circuits that operate to hold one input while sample a new input. The system of Brandt can be implemented using flash converters or any type of analog to digital converters and further operate at high speed and reduce power consumption. Therefore, any artisan having ordinary skill in the art would have been able to modify

Art Unit: 2819

the Shaw et al. by incorporating the teachings of Brandt to provide an improve analog to digital converter circuit.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claim 10 is rejected under 35 U.S.C. 102(b) as being anticipated by Shaw et al.(USP 4,218,675).

Shaw et al. disclose in Figure 1 an analog to digital converter that comprises an input circuit (analog input) a reference circuit (14), a first converter (comparator 12) that determines the most significant bits, a second converter (comparator 46) that determines the least significant bits; latch (44) that receives the output of the second comparator representative of the comparison of the input signal (analog input) with the reference voltage.

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Becker et al. (USP 6,285,095).

6. Becker et al. disclose in Figure a compensation circuit that comprises an array of capacitors, an array of switches and a memory for storing digital data (see col. 7, lines 18-32). Becker e t al. do not teach an array of memory elements. However, it would have been an obvious design choice to an artisan having working knowledge in circuit designs to substitute an array of memory circuit in place of a single memory circuit

Art Unit: 2819

based on the particular environment and system's requirements the memory circuit is to be used.

***Allowable Subject Matter***

8. Claims 4, 6, 15 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kao (USP 6,011,502) discloses a two-step analog to digital converter circuit.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peguy JeanPierre whose telephone number is (571) 272-1803 and the Examiner fax number is (571) 273-1803.

  
Peguy JeanPierre

Primary Examiner

April 16, 2004